Advanced Electronics Developed for NASA's Mars Exploration Program

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Abstract—Six electronic technologies under development for the Mars Technology Program are discussed. The scope of this set ranges from electronic packaging to microprocessors to power supply to communication technologies. An overview (motivation, objective, approach) of these six projects is presented, along with a comparison to the state-of-art. The overarching goal is to develop and mature these technologies to a point where the Mars Exploration Program can consider their use in a specific flight mission.

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1. INTRODUCTION

The Johns Hopkins University Applied Physics Laboratory (APL) is working with NASA to deliver six different electronics technologies to meet the Mars Exploration Program needs. Although these tasks are not part of a flight program, all products must be ready to support the 2009 Mars Science Laboratory (MSL) and the missions in the second decade of flight. Work began in fiscal year (FY) 2003, and each task will complete in FY 2005. NASA and APL chose the specific tasks jointly for their primary value to the NASA Mars Exploration Program (MEP), and also for their broader value to other Government space needs. A specific goal is to transfer these technologies to Industry so the broader Aerospace Community may access them.

The Mars Technology Program (MTP), a part of the NASA MEP, exists to develop technologies needed for future Mars missions. MTP is tightly focused on delivering products at a technology readiness level suitable for adoption by a flight program, with a specific goal of achieving Technology Readiness Level (TRL) 6[1] [1], [2]. The two principle program elements of MTP are the Focused Technology and the Base Technology Programs. The Focused Technology Program addresses technologies that are specific and critical to near-term missions, while the Base Technology Program addresses those technologies that are applicable for multiple missions and which can be characterized as longer term, higher risk, and high payoff technologies. [3]

The six MTP tasks were chosen for their high potential for insertion into a flight program. The focus was on the MSL, then on broader applicability to other Mars and NASA missions. Therefore, the schedule was driven by the 2009 MSL and the MEP second decade of flight. Throughout the development process APL worked closely with the NASA network of Jet Propulsion Laboratory (JPL) engineers connected to the Mars flight programs. In this manner, the relevancy of each task was ensured. Further, a flight insertion path was built into each task. These paths will be exercised as the technologies mature.

The six technologies discussed below are the Physics of Failure study of electronic packaging, a rad-hard microprocessor for actuator control, readout electronics for aeroshell sensors, a rad-hard power converter designed to be efficient at low loads, a Ka-band vector modulator to support future communications, and a synthesized low-mass ultra-stable oscillator for communications, navigation, and science applications. For each technology task, the following sections present an overview, state the objective and approach, compare the goals to the current state-of-art, and discuss the significance of the advancement.

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[1] TRL 6: System/subsystem model or prototype demonstrated in the relevant environment.

2. PHYSICS OF FAILURE STUDY

Long-lived, landed assets and rovers face a severe thermal environment on Mars. The current approach is to place the electronics in thermally controlled environments. This limits the design trade space, and capability. Therefore, future rover/lander designs will benefit from electronics that survive direct exposure to the surface thermal cycles. With night-time temperatures as low as -125C and neighboring components as warm as +85C, MSL electronics have to survive at least 500 thermal cycles – and be qualified for 1500 cycles. This is a significant challenge for electronic packaging technology. With partners JPL and University of Maryland Computer-Aided Life-Cycle Engineering (CALCE) Center, we are developing models of wire bond [2], [3], [4] die, and encapsulant failures likely encountered over long durations in the Martian environment. The Physics of Failure (PoF) approach develops an understanding of how the materials respond to thermal stress. The models created from this understanding guide the design and future accelerated testing of electronics. The POF study work complements such testing conducted at JPL in their Thermal Cycle Resistant Electronics program.

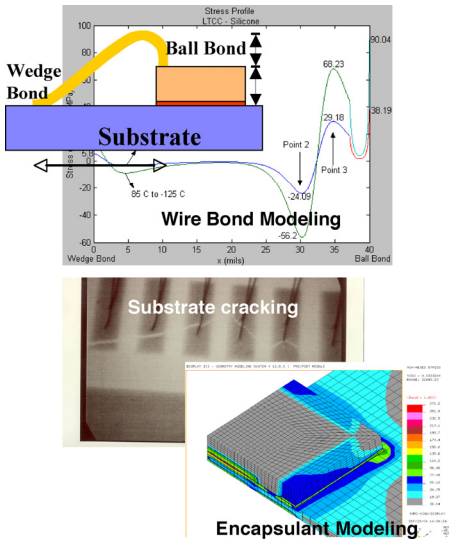

Figure 1 – A physics of failure study to electronic packaging includes material study and model development, to include wire bonds, die adhesives and encapsulants.

The severe temperature environment, both the low temperature and the daily temperature excursion (-125C to 85C) create challenges to designing the electronics for rovers and landers. For example, the eutectic solder material, die encapsulation materials, and adhesive materials can experience fatigue fracture at very low temperature; and the wire bonding process has not been tested at the extreme low temperature. The applicability of most electronic components and materials beyond the limited survival and functional temperature range is unknown. Any minor damage from one thermal cycle can grow to have major impact in the cyclical temperature environment the MSL will experience (500 life cycles, 1500 qualification cycles). The current military standards for electronics design and test can no longer provide sufficient reliability credits for the electronics exposed to such extreme low temperatures, and enduring the long mission duration with over 1500 cycles of temperature fluctuation. Potential failures induced by the unique environment of the Mars mission must be assessed to ensure long-term reliability of the electronics, which is crucial for the success of the entire mission.

This project was selected because current packaging standards cannot guarantee survival within the Martian surface environment. Further, there is little understanding of the failure mechanisms encountered within this environment. Without a PoF approach future flight programs are forced to rely upon a series of screening-tests to validate the design process. Instead, this project will develop the models needed to guide the design process and reduce risk.

To understand the root cause of failures of the electronics in the severe Mars temperature environment, a fundamental knowledge of material behavior and the impact on the electronics are crucial [5]. The physics-of-failure reliability assessment is a method used to identify possible failure sites, predict possible failure mechanisms, and assess service life of the electronics due to each of the failure mechanisms. Multiple failure mechanisms can occur simultaneously at the same failure site given the external 'stress' condition; the PoF approach allows identification of the dominant failure mechanism, permits 'damage' evaluation caused by each of the failure mechanism, and enables life prediction through principles of damage superposition.

The overall objective of this project is to identify possible failure mechanisms and access reliability of the electronics based on specific mission profile using the PoF approach, and to ensure survivability and functionality of the electronics through the entire Mars mission. The PoF approach also provides crucial guidelines in terms of material selection for the specific temperature range, electronic parts selection, interconnect material and process selection, and screening procedures, and proper accelerated life tests.

The study approach is summarized by:

- Material selection guidelines for low temperature application.
- Recommendation for parts selection, interconnect methods, and qualification methodology.
- Identification of various 'stress' environments for electronics. Electronics can be subjected to various levels of severity depends on the function,

location, and design.
- Identification of dominating failure mechanisms.
- Stress analysis and failure analysis for each failure mechanism using the PoF approach.
- Life prediction based on damage superposition.
- Provide guidelines for accelerated life tests.
- Recommendation for improvement of the long-term reliability of the electronics.

Ensuring long-term reliability of electronics in low temperature environments is crucial for enabling and achieving successful missions to Mars. The unique temperature environment requires new in-depth studies of the material selection criteria, electronic components screening and testing levels, assembly procedures, and testing procedures and levels that are typical and conventional to current space programs, so that proper modifications, enhancement, and changes can be recommended. Findings in this study can be extensively applied to future deep space missions with stringent low temperature environments.

3. RAD-HARD MICROPROCESSOR

A radiation-hardened mixed signal microcontroller (RHMC) for controlling motors, actuators, and instruments exposed to the Martian thermal environment is the focus of our second task. This RHMC is to have its own on-chip electrically eraseable programmable read-only memory (EEPROM), analog to digital (A/D) and digital to analog (D/A) converters, and needs to operate over the -125C to 30C temperature range[2]. Also, the microcontroller must withstand at least 100krad, be immune to latchup, and have very low susceptibility to other single event phenomena.

Remotely operated equipment including spacecraft and planetary rovers must control numerous actuators like motors, relays, and valves. Data on subsystem operating parameters must also be collected to monitor operation, diagnose faults, and calibrate sensors.

This task will develop a radiation tolerant microcontroller with on-chip non-volatile memory, mixed signal data acquisition circuits, and modest bit rate data network interface. The microcontroller will also be designed to withstand Martian surface temperature extremes. A distributed electronics architecture based on the microcontroller chip can implement low-level data acquisition and control functions. High data rate, low latency, interrupt servicing tasks poorly suited to large, high performance, on-board computers are executed by remote microcontroller based nodes optimized for those functions. Utilization efficiency of the large computers is enhanced and development, testing, and system integration are simplified. A flexible on-board data network interfaces many such acquisition/control nodes to other spacecraft resources. Functionality of those resources is less dependent on specific applications, enhancing reusability of previously designed subsystems. Network based interfaces also ease subsystem testing and reduce time and complexity of integrating subsystems into the completed system.

Several technologies that have not previously been combined on a single chip will be used to develop the microcontroller. Hence the microcontroller was at TRL 2[3] at the beginning of this project. However, most of the key contributing technologies are much more mature:

- Commercial chips with similar capability, to the microcontroller proposed here have been developed (TRL 4[4]), but with inadequate radiation tolerance;
- Intellectual property for implementing the microcontroller logic is readily available and is in widespread commercial use (TRL 4);
- Design techniques for building rad-hard mixed signal ASICs at commercial CMOS foundries have been developed and radiation tolerance has been verified (TRL 6-7[5]);
- Several of the key functions required by the microcontroller have been built and tested using radiation tolerant by design techniques including A/D, D/A, temperature sensor, radiation monitor, and network interface (TRL 5[6]);
- Prototype radiation tolerant EEPROM circuits that can be embedded in the microcontroller have been built and are now being characterized (TRL 3[7]); and
- Characterization of low temperature (-125C) operation of CMOS transistor device behavior is not widely available and will be performed by this task. Collected data will be used to design a mixed signal cell library design optimized for operation at low temperature and then used to develop the final version of the microcontroller (TRL 1[8]).

[2] The temperature range is narrowed from -125C to 85C to -125C to 30C to keep focus on low temperature operation.

[3] TRL 2: technology concept and/or application formulated.

[4] TRL 4: component and/or breadboard validation in laboratory environment.

[5] TRL 7: system prototype demonstrated in a space environment.

[6] TRL 5: component and/or breadboard validation in relevant environment.

[7] TRL 3: analytical and experimental critical function and/or proof of concept.

[8] TRL 1: basic principles observed and reported.

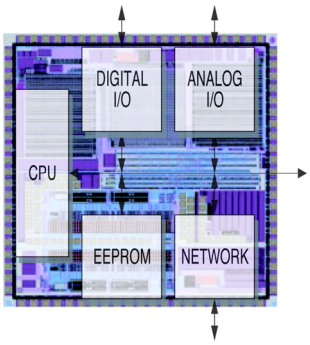

Figure 2 – The rad-hard processing unit consists of a single chip with on-board memory and peripherals

Development of this microcontroller is organized into five areas of effort:

- Definition of capabilities based on target applications;
- Design and validation of key circuits;
- Implementation of the complete microcontroller;
- Characterization of CMOS device behavior at low temperature; and
- Optimization of the microcontroller for low temperature operation.

Microcontroller capabilities will be defined based on potential applications including Mars Rover motor control and instrument mechanism control. The microcontroller instruction set architecture will be chosen based on IP availability, suitability for implementation with radiation tolerant by design techniques, availability of software development support, and user preferences.

Key circuits will be implemented in test chips to verify proper operation before design of the fully integrated microcontroller is completed. A test chip of the processor core will be built to verify proper use of the original IP and the computer aided engineering tool flow for translation from hardware description language to silicon for complex digital circuits. Mixed signal functions may also be prototyped with a test chip depending on similarity to existing APL designs. Finally, a test chip implementing a complete EEPROM subsystem will be built to verify that circuit's functionality and radiation tolerance. All circuits are expected to withstand >100 krads total dose exposure and be sufficiently immune to destructive single event effects for deep space missions. Non-destructive single-event-upset (SEU) immunity will be achieved by using majority-voting, or other techniques, for latches and memory where needed.

Microcontroller design including processor core, peripherals, and non-volatile memory will be completed after functionality of the key circuits has been evaluated. Prototype parts will be fabricated through the MOSIS Silicon Broker service and will be functionally verified. Radiation tolerance to both total dose and single event effects will be characterized and behavior over temperature variation will be measured. This prototype will verify design functionality, support initial software/hardware development, and enable earlier project use of the final microcontroller.

In parallel with development of the initial prototype microcontroller, operation of CMOS circuits over temperatures corresponding to the Martian surface environment will be characterized. However, low temperature effects at the package, board, and box level will not be addressed within this task (these issues are expected to be studied by the Physics of Failure ATD Task in collaboration with other JPL studies). Prior experience at APL and elsewhere has shown that CMOS transistors can function below -125C. However, predictions of cold behavior extrapolated from standard models may not be sufficiently accurate to support mixed signal circuit design. Performance of individual design elements (transistors and passives) at cold temperatures will be measured and circuit simulation model parameters will be determined. Circuit designs will be simulated over Mars surface temperature variations and modified to achieve acceptable performance. Test structures of cell designs optimized for low temperature operation will be fabricated and evaluated to validate circuit simulations. These cells will be used in the development of the microcontroller design for low temperature operation.

This effort includes the prototype design and verification phase of the development of an integrated circuit. Fabrication of the integrated circuit design plus preliminary temperature, radiation, and performance characterization are included. This task will develop a chip up to the state where activities related to flight fabrication (generation of formal worst case analysis, test vectors, formal documentation, etc.) could be initiated. Flight component manufacturing and qualification will not be performed by this task.

This microcontroller will impact of a wide variety of missions. The part will reduce system mass by replacing complex data acquisition harnessing with simple network interconnections. Power consumption is also likely to be reduced since the controller peripherals will use less current than most equivalent radiation tolerant components now in common use. The interface between main processor and data acquisition sensors and actuators occurs over an on-board network thus easing system integration, encouraging subsystem reuse, and supporting more flexible data acquisition subsystem design. Optimization over temperatures expected on the surface of Mars will enhance its suitability to Rover applications such as distributed motor control. The microcontroller will also have diverse instrument mechanism control and sensing applications.

4. AEROSHELL READOUT ELECTRONICS

The overall goal is to advance the knowledge of aeroshell performance, and improve the models by acquisition of actual flight data. To this end we are partnered with NASA Ames to provide a TRL6 minimum data acquisition system for the aeroshell temperature and heat-flow sensors under their development. The architecture is a flight proven processor board (Fig 3) and two sensor interface boards, one each for the foreshell and aftshell. The interface boards will use the TRIO Temperature Remote I/O chips developed at APL for NASA's X2000 program.

The risk associated with aeroshell design are currently mitigated by costly design margins (over 300% for aft-body aeroshells). By integrating sensors into aeroshells and collecting in situ data, models can be developed to guide low-mass designs. The high cost of aeroshell margin recently motivated NASA to direct the Mars Exploration Rover Opportunity to navigate to the debris of its own aeroshell (Fig 4). By turning its science instruments towards this activity NASA hopes to learn how the existing design performed.

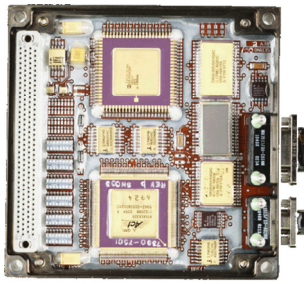

Figure 3 – The flight proven processor board for aeroshell electronics.

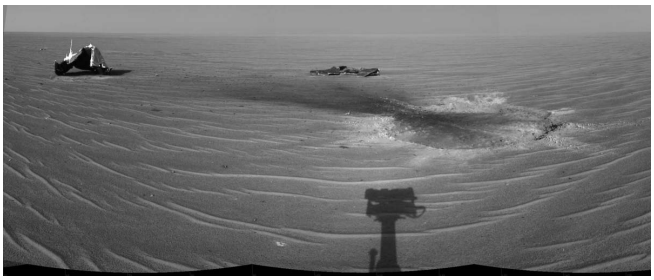

Figure 4 - Mars Exploration Rover leaves the Endurance Crater to examine its own aeroshell [10]

This task includes developing support electronics for the microSensor and Instrumentation Technology for AeroCapture (SITAC) program [11], funded by NASA's In Space Propulsion Program. A laboratory testbed version of the readout electronics and software have been developed and delivered to NASA Ames to measure the heat-flux sensor characteristics (eg. impedance) and validate the front-end design. These characteristics drive the design of the flight-prototype readout electronics. The electronics must be capable of reading out approximately 64 temperature sensors multiple times per second (approximately 10 Hz) for a period of time compatible with atmospheric entry (approximately 165 seconds), and storing the digitized data in an internal memory. The data would then be presented to a spacecraft/host interface at a later time for readout. This approach minimizes the number of wires coming from the aeroshell to the electronics: 4 wires from the deployed shield accommodate power, ground and all the enclosed sensors. This reduces deployment risk and the amount of heat that flows from the aeroshell into the spacecraft interior. The "black box" will be brought to at least TRL 6 maturity during this effort.

The X2000 investment in TRIO and TAS will be leveraged to create the three board Aeroshell TRIO Assembly Slice (ATAS) Unit. There will be two miniaturized TAS boards, each with several TRIO-C parts to read the temperatures (developed for X2000 and based upon APL's TRIO flown on MESSENGER), and a field-programmable gate array (FPGA). Also a flight-ready processor board (a copy of a NASA New Horizon's data processing unit) will be used. The ATAS hardware will be tested in an appropriate simulated space environment for TRL6 readiness. The prototype ATAS unit will then be delivered to support the Ames Arc Jet facility tests of the Aeroshell sensors.

NASA Ames presently has no flight-heritage readout electronics for the SITAC sensors. This work is motivated by the desire to bring an entire aeroshell measurement system (material, sensors, and electronics) to a mature readiness level.

5. LOW POWER DC/DC CONVERTER

NASA seeks development of DC-DC Power Converters designed to be rad-tolerant and efficiently optimized for low power applications (<5W loads). Commercial grade DC-DC power converters can leverage ultra low power CMOS integrated circuits to achieve very high power conversion efficiency even for low power applications. Unfortunately, space grade DC-DC converters generally cannot take advantage of these low power CMOS ICs because of their poor tolerance for radiation. Thus, space grade DC-DC converters have historically relied on bipolar ICs to obtain the requisite radiation performance. The cost is a significant increase in power consumption for the DC-DC converter over comparable commercial grade products. In many cases, this increase represents only a minute fraction of the total system power budget and is of little consequence. But for those subsystems that consume relatively little power (approximately 5W or less), the DC-DC converter losses can be significant. As the next generation of space electronics continues to drive toward lower power consumption, the problem will only get worse.

This task therefore seeks to enable the development of radiation tolerant DC-DC converters that can efficiently operate in such low power applications. The benefits of achieving this goal are substantial:

- Lower DC-DC power consumption for increased battery life and mission duration
- Enables distributed power system architectures for increased robustness and less susceptibility to mission critical single point failures
- Simplifies system test and integration by reducing the number of subsystems interacting with a common power supply

Further, these benefits are potentially applicable to a wide range of components and subsystems across many different mission profiles. Scientific instruments, distributed sensors and actuators, telecommunications boxes, power systems, and more could potentially benefit from the results of this task.

Our approach is to first develop a new Pulse Width Modulator integrated circuit using "rad-hard by design" techniques to simultaneously achieve very low power consumption and high tolerance for radiation. The PWM circuit was chosen because it is the command and control "smarts" behind nearly all modern DC-DC converters and generally dominates the converter's power consumption for light output loads. By significantly reducing its power consumption, we can affect a significant increase in overall DC-DC converter efficiency for low load applications (e.g. less than 5W). Table 1 communicates the advantage expected relative to the state-of-practice PWMs.

Table 1. PWM Chip Performance

PWM Chip	Typical Power Consumption	Total Ionizing Dose
UC1843	110 – 300 mW	100 krads
UC1800	5 – 10 mW	Less than 3 krads
LT1170	60 – 120 mW	3 – 6 krads
MAX5053	3 – 5 mW	Less than 3 krads
Mars MTP	**5 – 10 mW**	**100 – 300 krads**

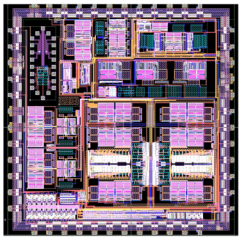

Figure 5 – The PWM chip is designed for efficient, DC/DC converters designed for loads under 5W.

In defining the detailed specifications for the PWM chip, we solicited input from a wide range of potential users to maximize the chip's applicability. At a minimum, the chip will contain all the components necessary to perform PWM control: error amplifier, oscillator, precision voltage reference, control logic, and drive circuitry. In addition, several features will be included to increase the appeal and utility of the final product: an uncommitted op-amp for signal conditioning, dual push-pull outputs with break before make circuits, user selectable 50% or 100% maximum duty cycle limit, and a power good output indicator are just a few examples.

Prototype PWM chips will be fabricated and tested in a laboratory environment to quantify performance metrics and verify functionality. The prototype parts will also be tested over a range of thermal and radiation environments representative of the Mars Exploration Program environment to bring the PWM prototypes up to NASA TRL 6.

Additionally, a prototype DC-DC converter will be designed and built based on the new PWM chip. The prototype will be used to demonstrate the capabilities of the new PWM chip within the context of an overall DC-DC converter (efficiency, regulation, transient response, etc.)

The second phase of our task focuses on bringing the new PWM chip to market and supporting its sale to the wider space electronics community. For this we have partnered with Aeroflex Microelectronic Solutions, Inc. who will be responsible for publishing marketing and sales support, manufacturing and qualifying flight parts. By making the PWM chip available to the wider space design community in this way, we hope to improve the efficiency and robustness of DC-DC converters, systems, and components across the board.

6. KA-BAND VECTOR MODULATOR

The fifth MTP task at APL is the development of a Ka-Band Monolithic Microwave Integrated Circuit (MMIC) to support JPL's advanced transponder designs. These designs need the equivalent of both a linear modulator and a quadrature phase shift keying (QPSK) modulator. To serve both these functions, we are developing a Ka-Band vector modulator chip.

This MMIC development will leverage APL's extensive MMIC design experience, which includes a 4-bit Ka-band phase shifter previously developed under NASA Advanced Technology Development funding. The MMIC chip to be developed represents a key Ka-band chip in a suite of MMICs needed for the next generation of Mars transponders and transceivers.

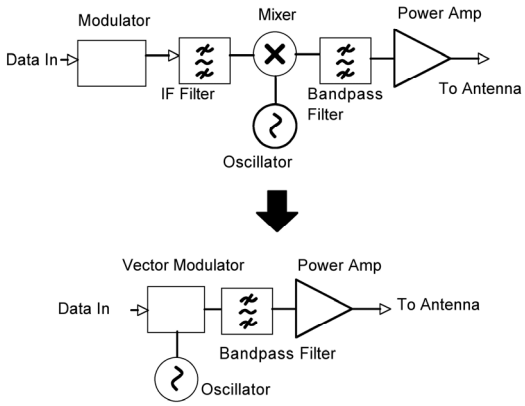

Figure 6 – A direct Vector Modulator enables simpler architectures, reducing RF hardware and cost.

There are a wide range of Mars mission concepts that would benefit from the MMIC development. The radio developments needed to support future Mars missions require more than the typical "off-the-shelf" solutions. In addition to the Mars relay communication orbiter, MMICs could also be used on in-situ sub-surface, surface or near-surface missions such as balloon or glider missions where mass, size, and power consumption are critical. The simplified and miniaturized MMIC approach also lowers mission risk by providing higher reliability than the current multi-chip module (MCM) approach and offers lower mass along with increased assembly, integration and test yield. The MMIC approach provides a big payoff in mass, size, cost and reliability and will materially contribute to enabling certain missions where these factors are critical.

APL is employing its typical approach to MMIC circuit design such as use of linear and nonlinear simulators, use of planar ElectroMagnetic simulators, and design-rule checking. Variations of individual sub-circuits (combiners, multipliers) were included in an initial foundry pass (Fig. 7) to facilitate troubleshooting and to calibrate the circuit modeling. Following the initial "test chip" a first pass vector modulator was fabricated along with individual test sub-circuits as room allowed (Fig. 8). The overall vector modulators are expected to require no more than two full passes through the foundry to yield designs with suitable performance for the space-flight production.

The primary goal is to research and develop to TRL-6 a Ka-Band Vector Modulator MMIC. After the completion of the first foundry pass for this chip, APL will assess the effort required to complete the MMIC described above.

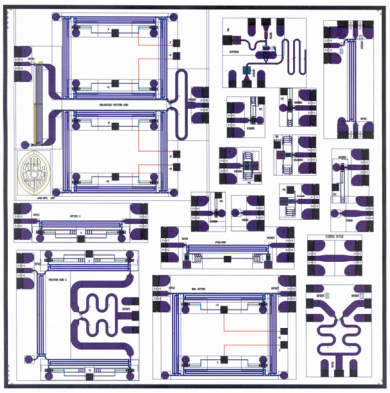

Figure 7 – Both a narrow and broad band design are under study for the Ka-Band Vector Modulator MMIC

Deliverables will include working prototype MMIC chips. In addition, documentation of the final design and performance will be provided. A period of technology transfer is baselined to insure that industry partners are fully prepared for producing and screening high-reliability versions of these custom MMIC designs. This technology transfer effort includes documentation of test set-ups and procedures for electrical screening that a foundry or suitable third party vendor could use as a basis for establishing their own test procedures for electrical testing of space-qualified flight devices. This advanced technology development concludes with the technology transfer effort. The remaining tasks required to produce space-qualified flight parts include: generation of program specific documentation such as NSPAR (Non-standard part approval requests), non-recurring engineering of burn-in boards and test fixtures, and generation of assembly instructions or travelers. It is anticipated that these tasks along with all electrical and environmental screening and visual inspections will be performed by either the MMIC foundry or a suitable third party vendor, not by APL.

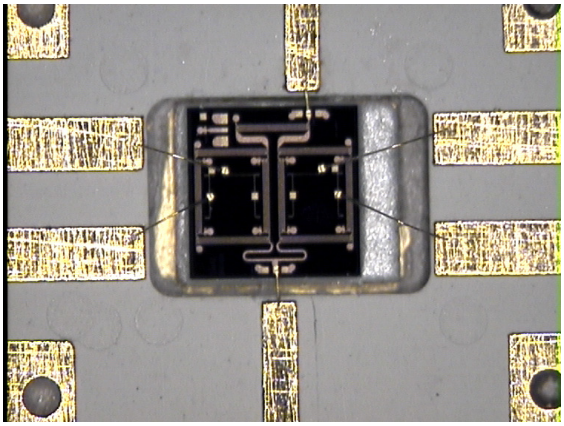

Figure 8 - Broadband 1st pass Ka-band Vector Modulator in a test package.

7. SYNTHESIZED ULTRA-STABLE OSCILLATOR

Finally, APL is developing a synthesized, micro-USO (ultra-stable oscillator). This ovenized, crystal oscillator will incorporate a frequency synthesizer to enable standard 5MHz resonators to realize in-flight tuning across the channels in the Deep Space Network – with science grade RF performance. Further, we intend to significantly reduce the mass and power characteristics from those USO's flying on NASA's GRACE and Cassini-Huygens spacecraft.

A synthesized ultra-stable oscillator (USO) is being developed to provide a frequency reference for transponders and other on-board users on future Mars missions [12]. The frequency reference is to be stable enough for radio-science and navigation applications, but also must be electronically tunable over a limited band. Fixed frequency USOs with the desired stability have been demonstrated on prior flight programs such as Cassini and Mars Global Surveyor. Synthesizer technologies have also been demonstrated in flight, but not with the desired stability. The present technology readiness level is 3.

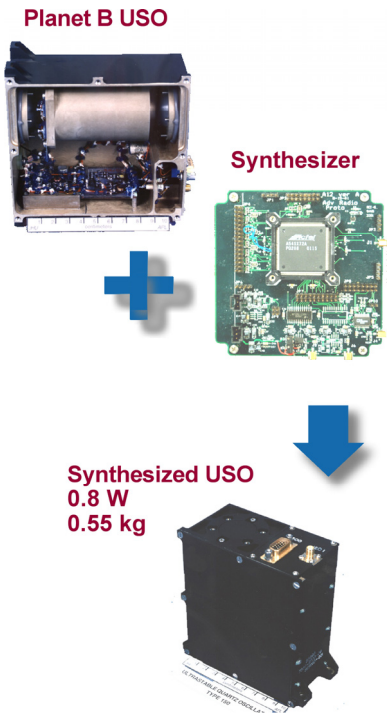

Figure 9 – The Synthesized USO will combine APL's proven science-grade ovenized quartz oscillators with a synthesizer, while reducing mass and power requirements.

The objective is to reduce spacecraft development time and provide communications channel assignment flexibility. Then the synthesized USO can be manufactured and delivered to spacecraft integration prior to channel assignment. Final channel selection is made by electronically tuning the transponder reference USO.

Several technologies are being considered that include quartz crystal oscillators, voltage controlled oscillators, direct digital synthesis, and mix/multiply/divided schemes. Computer models will be developed to simulate the expected performance of the candidate technologies, followed by breadboard tests, and ultimately engineering model tests.

This task will potentially reduce mission cost by reducing overall schedule length. The reference oscillator is typically a long lead item, and can impact spacecraft schedule time if its manufacture cannot begin until after the channel assignment. The synthesized USO will alleviate this impact. Some economy of scale can also be realized with the procurement of several identical synthesized USOs instead of the typical two unique USOs per spacecraft.

8. SUMMARY

Six electronic technology projects were carefully chosen for their potential impact on the Mars Exploration Program, and funded by the Mars Technology Program. In their last year of development, each is on track to reach TRL 6 the end of FY05. The physics of failure study will guide the design of future electronics used on the Martian surface. The microprocessor is poised to withstand the cold of Mars and control actuators and instruments. Aeroshell readout electronics based on flight proven components can collect and return valuable aeroshell performance data, so future designs can be improved. Communications will be improved at Ka-band with a vector modulator MMIC chip to support new deep space transponders and transceivers. The Synthesized Ultra-Stable Oscillator will provide access to all Deep Space Network channels while reducing USO mass and power requirements.

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Physics of Failure..... Sharon Ling
Rad-Hard Microprocessor..... Marty Fraeman
Aeroshell Readout Electronics.. Chuck Schlemm
Low Power DCDC Converter... Geoffrey Marcus

Ka-Band Vector Modulator.....John Penn
Synthesized Ultra-Stable Osc ....Bob Wallis

Barry Tossman manages the six projects as Program Manager, and Robert Gold directs the overall effort. The cooperation and support of NASA Ames is also noted and greatly appreciated in advancing the aeroshell electronics.

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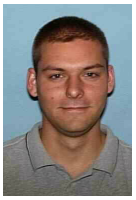

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